

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A method of exporting from a data
2 processor emulation information including emulation control
3 information and emulation data, comprising:
4 arranging the emulation information into fixed length
5 information blocks;
6 outputting a sequence of the information blocks from the data
7 processor via a plurality of terminals of the data processor;
8 said arranging step including providing some of the
9 information blocks of the sequence with relative proportions of
10 emulation control information and emulation data that differ from
11 the relative proportions of emulation control information and
12 emulation data in other blocks of the sequence;
13 storing comparison data;
14 comparing respective sections of emulation data with the
15 stored comparison data; and
16 wherein the emulation control information in one of the
17 information blocks includes a compression map indicative of whether
18 the sections of the emulation data match the stored comparison
19 data.

2 to 4. (Canceled)

1 5. (Previously Presented) A method of exporting from a data
2 processor emulation information including emulation control
3 information and emulation data, comprising:
4 arranging the emulation information into fixed length
5 information blocks, the emulation data in one of the information
6 blocks includes bits indicating whether the data processor

7 performed data processing operations during a corresponding clock
8 cycle;
9 outputting a sequence of the information blocks from the data
10 processor via a plurality of terminals of the data processor; and
11 said arranging step including providing some of the
12 information blocks of the sequence with relative proportions of
13 emulation control information and emulation data that differ from
14 the relative proportions of emulation control information and
15 emulation data in other blocks of the sequence.

6 to 12. (Canceled)

1 13. (Previously Presented) An integrated circuit device,
2 comprising:
3 a data processing portion for performing data processing
4 operations;
5 an emulation information collector coupled to said data
6 processing portion for receiving emulation data therefrom, said
7 collector operable for arranging the emulation data and associated
8 emulation control information into fixed length information blocks;
9 a plurality of terminals coupled to said collector for
10 permitting said collector to communicate with an emulation
11 controller located externally of said integrated circuit device;
12 said collector operable for providing to said terminals a
13 sequence of said information blocks to be output to the emulation
14 controller, said collector further operable for providing some of
15 the information blocks of the sequence with relative proportions of
16 emulation control information and emulation data that differ from
17 the relative proportions of emulation control information and
18 emulation data in other blocks of the sequence;
19 a comparison data register storing comparison data;
20 a comparator connected to said comparison data register and
21 receiving emulation data generating an indication of a match

22 between corresponding sections of said comparison data and said
23 emulation data; and
24 wherein the emulation control information in one of the
25 information blocks includes a compression map indicative of whether
26 the sections of the emulation data match the stored comparison
27 data.

14 to 16. (Canceled)

1 17. (Currently Amended) An integrated circuit device of
2 comprising:
3 a data processing portion for performing data processing
4 operations;
5 an emulation information collector coupled to said data
6 processing portion for receiving emulation data therefrom, said
7 collector operable for arranging the emulation data and associated
8 emulation control information into fixed length information blocks,
9 the emulation data in one of the information blocks includes bits
10 indicating whether the data ~~processor~~ processing portion performed
11 data processing operations during a corresponding clock cycle;
12 a plurality of terminals coupled to said collector for
13 permitting said collector to communicate with an emulation
14 controller located externally of said integrated circuit device;
15 and
16 said collector operable for providing to said terminals a
17 sequence of said information blocks to be output to the emulation
18 controller, said collector further operable for providing some of
19 the information blocks of the sequence with relative proportions of
20 emulation control information and emulation data that differ from
21 the relative proportions of emulation control information and
22 emulation data in other blocks of the sequence.

18 to 27. (Canceled)